REMARKS

Further to the Preliminary Amendment filed March 7, 2002, the specification has been further amended for clarification.

It is also noted that reference was made that claim 46 was amended in the Preliminary Amendment, when in fact reference should have been made that claims 26 to 28 were amended.

Entry of this Second Preliminary Amendment and examination of this application on its merits is respectfully requested.

Respectfully submitted,

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(Seventy-ninth embodiment)

The bottom-gate TFT array substrate according to the seventy-eighth embodiment may be such that the oxide film of the side surfaces of the gate electrodes is an anodic oxide film.

(Eightieth embodiment)

The bottom-gate TFT array substrate according to the seventy-eighth embodiment may be such that part of each source segmented wiring line has a five-layered structure composed of a gate wiring line metal film, a gate insulating film, a semiconductor film, a contact metal film layer, and a metal electrode film.

(Eighty-first embodiment)

The bottom-gate TFT array substrate according to the seventy-eighth embodiment may be such that the contact electrode metal is formed between the semiconductor film and a source electrode and between the semiconductor film and a drain electrode.

(Eighty-second embodiment)

The bottom-gate TFT array substrate according to the seventy-eighth embodiment may be such that the source segmented wiring lines are severed by the gate wiring lines, and segments of each source segmented wiring line are interconnected together on the gate wiring lines by a contact electrode metal and the metal electrode.

(Eighty-third embodiment)

The bottom-gate TFT array substrate according to the seventy-eighth embodiment may be such that part of the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer.

the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

(Ninety-first embodiment)

The liquid crystal display device according to the ninetieth embodiment may be such that at least part of the TFT array is covered with a passivation film.

(Ninety-second embodiment)

The liquid crystal display device according to the ninety-first embodiment may be such that the passivation film is an inorganic substance.

(19) A nineteenth aspect of the present invention (ninety-third to ninety-fifth embodiments) includes the following.

(Ninety-third embodiment)

There is provided a method of fabricating a liquid crystal display device comprising: fabricating a first bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact metal film layer on a surface of an insulating substrate; by photolithography, sequentially etching the contact metal film layer, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes; forming a metal electrode film; by photolithography, sequentially etching part of the metal electrode film, the contact metal film layer, and the semiconductor film, using a second pattern; and forming second

comb-shaped pixel electrodes, using a third pattern, with a passivation film disposed between the second comb-shaped pixel electrodes and the substrate; forming an alignment film on the first substrate; forming an alignment film on a surface of a color filter side of a second color filter substrate; adhering and fixing the ~~the~~ first and second substrates at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and injecting a specified liquid crystal between the first and second substrates.

(Ninety-fourth embodiment)

The fabrication method according to the ninety-third embodiment may further comprise, after the formation of the second comb-shaped pixel electrodes, covering at least part of each second comb-shaped pixel electrode by a passivation film.

(Ninety-fifth embodiment)

The fabrication method according to the ninety-third embodiment may be such that the passivation film is a silica film or a silicon nitride film.

(20) A twentieth aspect of the present invention (ninety-sixth and ninety-seventh embodiments) includes the following.

(Ninety-sixth embodiment)

There is provided a bottom-gate TFT array substrate comprising source segmented wiring lines, gate electrodes, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel electrode group, the bottom-gate TFT array substrate wherein: at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized;

semiconductor film, an amorphous silicon (i-type a-Si) film layer not containing impurities and an amorphous silicon (n+a-Si) film layer containing an n-type impurity to 50 nm and 50 nm, respectively. Finally, a Ti metal film, serving as a contact metal film layer, was vapor deposited by sputtering to a film thickness of about 100 nm. Thereafter, a first resist pattern for the first photolithography, which includes first comb-shaped pixel electrodes, was formed by a conventional method.

Then, the contact metal film layer (Ti), the n+a-Si film layer, the i-type a-Si film layer, the gate insulating film layer (SiN_x film), and the G-S metal film layer (Al–Zr film) were sequentially etched, thereby forming a first pattern including a gate electrode or a gate wiring line, a source segmented wiring line, a gate insulating film layer, and a semiconductor film, which were stacked, and a first comb-shaped pixel metal electrode 251.

Next, the gate electrode, the gate wiring line, and the first comb-shaped pixel metal electrode 251 were anodically oxidized in an electrolyte using ammonium borate and having a pH in the neighborhood of 7, to form insulating films, mainly composed of Al_2O_3, on the side surfaces of the pattern.

Further, a metal (Al) electrode film was vapor deposited by sputtering to a film thickness of about 100 nm. The metal electrode film was to be connected to source regions and to second comb-shaped pixel metal electrodes connected to drain regions and was to connect together segments of each severed source segmented wiring line.

Subsequently, a second resist pattern for the second photolithography was formed by a conventional method. Then, part of the metal electrode

film, the contact electrode metal, and the n+a-Si film ~~206'~~ on the gate electrode were sequentially etched away through to the i-type a-Si film, thus forming channel regions. The source segmented wiring line ~~209'~~ was connected to a source region by a portion of the contact electrode metal and a metal electrode, and a second comb-shaped pixel metal electrode was connected to a drain region by a portion of the contact electrode metal.

At this point, the source segmented wiring lines~~—and~~, which had been previously severed, were connected together on the gate wiring line by the metal electrode film pattern via a portion of the contact electrode metal.

Finally, by using printing and baking a silica passivation film 217 of 300 nm was formed so as to cover the TFTs, and subsequently using this silica passivation film pattern as a mask, portions of the i-type a-Si film and the SiN_x film on the gate electrode metal, which are to be connected to external driving circuitry, were etched away, thus producing a TFT array substrate 253 applicable to in-plane switching (IPS) mode liquid crystal display devices (Figs. 22(a) and 22(b)).

Here, by simultaneously etching portions that are to be formed into gate wiring lines, gate electrodes, and first comb-shaped pixel electrodes, it was possible to fabricate a TFT array substrate for the IPS mode device, without additional masks.

In addition, carrying out the step of forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film made it possible to fabricate a TFT array substrate having excellent stability.

Moreover, by sequentially forming the gate wiring line metal film, the

substrate and the gate wiring line metal film, it was possible to prevent impurities migrating from the substrate from diffusing, providing a TFT array substrate with high reliability.

Example 2-6

The actual fabrication process of an IPS mode liquid crystal display device using the above-described TFT array substrate is described.

First, there were provided a TFT array substrate for the IPS mode device, similar to that of Example 2-5, fabricated using two masks, more specifically, a first TFT array substrate including a first comb-shaped electrode group and a second comb-shaped electrode group arranged in a matrix and a transistor group that drives the second comb-shaped electrode group; and a color filter substrate including a second color filter substrate group placed opposite to the first and second electrode groups. Over each of the substrates, by a conventional method, a polyimide resin was applied and cured, and the resulting films were subjected to rubbing, thus producing liquid crystal alignment films.

Next, the first and second substrates were arranged such that their respective alignment films oppose one another, thus producing a cell having a gap of about 5 microns created by spacers and adhesives. Thereafter, a nematic liquid crystal was injected between the first and second substrates, and polarizers were then arranged so as to have a crossed Nicols relation, thus completing a display device.

Such a device was capable of displaying images by driving each transistor using video signals while lighting, using the backlight from the

200 nm. Subsequently, a SiN_x film, serving as a gate insulating film, was deposited by plasma enhanced CVD to 150 nm, followed by, as a semiconductor film, an amorphous silicon (i-type a-Si) film not containing impurities and an amorphous silicon (n+a-Si) film containing an n-type impurity to 200 nm and 50 nm, respectively. Then, a first resist pattern for the first photolithography, which includes first comb-shaped pixel electrodes, was formed by a conventional method.

Thereafter, the n+a-Si film, the i-type a-Si film, the SiN_x film, and the Al-Zr film were sequentially etched, thereby forming a first pattern including a gate electrode or a gate wiring line, a source segmented wiring line, a gate insulating film layer, and a semiconductor film, which were stacked, and a first comb-shaped pixel electrode 261.

Next, the gate electrode, the gate wiring line, and the first comb-shaped pixel electrode 261 were anodically oxidized in an electrolyte of ammonium borate to form insulating films, mainly composed of Al_2O_3, on the side surfaces of the pattern.

Further, a contact metal film layer (Ti) and a metal electrode film composed of an aluminum film (Al) were vapor deposited by sputtering to film thicknesses of about 50 nm and 100 nm, respectively. The contact electrode metal film and the metal electrode film were to be connected to source regions and to second comb-shaped pixel metal electrodes connected to drain regions and were to connect together segments of each severed source segmented wiring line.

Subsequently, a second resist pattern for the second photolithography, which includes second comb-shaped pixel metal electrodes, was formed by a

conventional method. Then, part of the metal electrode film, the contact metal film layer (Ti), and the n+a-Si film on the gate electrode were sequentially etched away, thus forming channel regions. The source segmented wiring line ~~209~~ was connected to a source region by a portion of a contact metal film layer (Ti) and a metal electrode film pattern, and a second comb-shaped pixel metal electrode 262 was connected to a drain region by a portion of the contact electrode metal.

At this point, segments of the source segmented wiring line, which had been previously severed, were connected together on the gate wiring line by the portion of the contact metal film layer (Ti) pattern and the metal electrode film pattern.

Finally, by using printing and baking a passivation film of 300 nm was formed so as to cover the TFTs, and subsequently using this silica passivation film pattern as a mask, portions of the oxide film on the gate electrode metal which were to be connected to driving circuitry were etched away, thus producing a TFT array substrate 263 having the second comb-shaped pixel metal electrodes in the pixel portions (Figs. 23(a) and 23(b)).

Here, when the semiconductor film had a two-layered structure composed of an i-type layer and an n-type layer and part of the n-type layer was etched to the i-type layer, it was possible to fabricate a TFT array substrate at low cost without additional masks.

Further, by forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film, it was possible to prevent impurities generating from the substrate from diffusing, allowing

fabrication of a TFT array substrate with high reliability.

When the gate wiring line metal film, the gate insulating film, and the semiconductor film were sequentially formed, contamination of the channel portions was kept to a minimum, allowing fabrication of a TFT array substrate having stable Vt.

In the step of oxidation, by carrying out anodic oxidation in a neutral solution, it was possible to fabricate a TFT array substrate having few pinholes and little leakage current.

Moreover, when part of the TFT array substrate was covered, using a sol-gel method, by a passivation film composed of silica or a silica-containing inorganic substance, it was possible to fabricate a TFT array substrate with high reliability.

Example 2-8

The actual fabrication process of a liquid crystal display device using the above-described TFT array substrate is described.

First, there were provided a TFT array substrate for the IPS mode device, similar to that of Example 2-7, fabricated using two masks, more specifically, a first TFT array substrate including a first comb-shaped electrode group and a second comb-shaped electrode group arranged in a matrix and a transistor group that drives the second comb-shaped electrode group; and a second color filter substrate including a color filter group placed opposite to the first and second electrode_groups. Over each of the substrates, by a conventional method, a polyimide resin was applied and cured, and the resulting films were subjected to rubbing, thus producing

liquid crystal alignment films.

Next, the first and second substrates were arranged such that their respective alignment films oppose one another, thus producing a cell having a gap of about 4 microns created by spacers and adhesives. In addition, a nematic liquid crystal was injected between the first and second substrates, and two polarizers were then arranged so as to have a crossed Nicols relation, thus completing a display device.

Such a device was capable of displaying images by driving each transistor using video signals while lighting, using the backlight from the backside. Here, the device achieved a wide viewing angle of 160° horizontally and vertically with a contrast of 10.

Here, after the step of fabricating the TFT array substrate prior to the formation of the alignment films, by carrying out the step of covering at least part of the TFT array substrate by a passivation film such as silica, it was possible to fabricate a liquid crystal display device with high reliability.

Furthermore, when the metal electrode and the contact metal electrode were formed in a single layer with the same material, it was possible to further simplify the process.

Example 2-9

In a manner similar to that described in Example 2-1, a transparent glass substrate that had been thoroughly cleaned in advance was prepared, and a silica (SiO_2) film, serving as an undercoat film layer, was deposited by CVD to 0.4 microns. Then, an Al–Zr (97:3) alloy, serving as a G-S metal film layer for gate electrodes, gate wiring lines, and source segmented

conventional method. Then, part of the transparent conductive film, the contact electrode, and the n+a-Si film on the gate electrode were sequentially etched away through to the i-type a-Si film, thus forming channel regions. The source segmented wiring line was connected to a source region by a portion of the contact electrode metal and a metal electrode, and the first comb-shaped pixel metal electrode 271 was connected to a drain region by a portion of the contact electrode metal.

At this point, the source segmented wiring lines—~~and~~, which had been previously severed, were connected together on the gate wiring line by the metal electrode via a portion of the contact electrode metal.

Subsequently, a silica passivation film of 300 nm was formed by printing and baking, using a sol-gel method, so as to cover the TFTs. Thereafter, using this silica passivation film pattern as a mask, portions of the i-type a-Si film and the SiN_x film on the gate electrode metal, which are to be connected to external driving circuitry, were etched away.

An Al–Zr alloy was then vapor deposited on the entire surface to a film thickness of 150 nm, and using a photomask having a second comb-shaped electrode pattern, a second comb-shaped pixel metal electrode 272 was formed, thus producing a TFT array substrate 273 applicable to IPS mode transmissive liquid crystal display devices, with the use of three photomasks (Figs. 24(a) and 24(b)).

Here, when the semiconductor film had a two-layered structure composed of an i-type layer and an n-type layer and part of the n-type layer was etched to the i-type layer, it was possible to simplify the TFT process.

In addition, forming an undercoat film between the surface of the

insulating substrate and the gate wiring line metal film made it possible to fabricate a TFT array substrate having stable characteristics.

When at least the gate wiring line metal film, the gate insulating film, and the semiconductor film were sequentially formed, it was possible to prevent contamination of the channel interfaces.

In the step of oxidation, by carrying out anodic oxidation, it was possible to form an insulating film having few pinholes, allowing fabrication of a TFT array substrate having little gate leakage.

Here, when the oxide films of the side surfaces of the gate electrodes were formed of anodic oxide films, it was possible to fabricate a TFT array substrate having excellent leakage characteristics.

Furthermore, when part of the source segmented wiring line had a five-layered structure composed of the gate wiring line metal film, the gate insulating film, the semiconductor film, the contact ~~electrode~~ metal film layer, and the metal electrode film, it was possible to reduce the resistance of the source segmented wiring line, allowing fabrication of a TFT array substrate having few variations in characteristics.

When a contact electrode metal was formed between the semiconductor film and the source/drain electrodes, it was possible to fabricate a TFT array substrate having little internal resistance.

Moreover, when segments of each source segmented wiring line, which had been severed by the gate wiring lines, were interconnected together on the gate wiring lines by the contact electrode metal and the metal electrode, it was possible to fabricate a TFT array substrate having a low resistance of the source segmented wiring line.

When part of the semiconductor film had a two-layered structure composed of an i-type layer and an n-type layer, it was possible to omit the step of diffusing an n-type impurity.

Forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film made it possible to minimize the influence of the substrate deformation.

Example 2-10

The actual fabrication process of a liquid crystal display device using the TFT array substrate produced in the foregoing Example 2-9 is described.

First, there were provided a TFT array substrate, similar to that of Example 2-9, fabricated using two masks, more specifically, a first TFT array substrate including a first comb-shaped electrode group and a second comb-shaped electrode group arranged in a matrix and a transistor group that drives the first comb-shaped electrode group; and a second color filter substrate including a color filter group placed opposite to the first and second comb-shaped electrode groups. Over each of the substrates, by a conventional method, a polyimide resin was applied and cured, and the resulting films were subjected to rubbing, thus producing liquid crystal alignment films.

Next, the first and second substrates ~~and~~ were arranged such that their respective alignment films oppose one another, thus producing a cell having a gap of about 5 microns, which is created by spacers and adhesives. Thereafter, a TN liquid crystal was injected between the first and second substrates, and polarizers ~~and~~ were then arranged so as to have a

crossed Nicols relation, thus completing a display device.

Such a device was capable of displaying images by driving each transistor using video signals while lighting, using the backlight from the backside. Here, the device achieved a wide viewing angle of 160° horizontally and vertically with a contrast of 210.

Here, after the step of fabricating the TFT array substrate prior to the formation of the alignment films, by carrying out the step of covering at least part of the TFT array substrate by a passivation film such as silica, it was possible to fabricate a liquid crystal display device with high reliability.

Example 2-11

In a manner similar to that described in Example 2-8, a transparent glass substrate that had been thoroughly cleaned in advance was prepared, and a silica (SiO_2) film, serving as an undercoat film layer, was deposited by CVD to 0.4 microns. Then, an Al–Zr (97:3) alloy, serving as a G-S metal film layer for gate electrodes, gate wiring lines, and source segmented wiring lines, was vapor deposited by sputtering to a film thickness of about 200 nm. Subsequently, a SiN_x film, serving as a gate insulating film layer, was deposited by plasma enhanced CVD to 150 nm, followed by, as a semiconductor film, an amorphous silicon (i-type a-Si) film not containing impurities and an amorphous silicon (n+a-Si) film containing an n-type impurity to 50 nm and 50 nm, respectively, and then a first resist pattern for the first photolithography was formed by a conventional method.

Thereafter, the n+a-Si film, the i-type a-Si film, the SiN_x film, and the Al–Zr film were sequentially etched, thereby forming a first pattern

including a gate electrode or a gate wiring line, a source segmented wiring line, a gate insulating film layer, and a semiconductor film which were stacked.

Next, the gate electrode and the gate wiring line were anodically oxidized in an electrolyte using ammonium borate and having a pH in the neighborhood of 7, to form insulating films, mainly composed of Al_2O_3, on the side surfaces of the pattern.

Further, a Ti metal film, serving as a contact metal film layer, was vapor deposited by sputtering to a film thickness of about 100 nm, and subsequently an Al–Zr film, serving as a metal electrode film, was vapor deposited by sputtering to a film thickness of about 100 nm. The contact metal film layer and the metal electrode film are to be connected to source regions and to first comb-shaped pixel metal electrodes connected to drain regions, and to connect together segments of each severed source segmented wiring line.

Thereafter, a second resist pattern for the second photolithography, which includes a first comb-shaped electrode pattern, was formed by a conventional method. Subsequently, part of the transparent conductive film, the contact metal film layer, and the n+a-Si film on the gate electrode were sequentially etched away through to the i-type a-Si film, thus forming channel regions. The source segmented wiring line was connected to a source region by a portion of the contact electrode metal and a metal electrode, and the first comb-shaped pixel metal electrode 281 was connected to a drain region by a portion of the contact electrode metal.

At this point, the source segmented wiring lines—~~and~~, which had been

previously severed, were connected together on the gate wiring line by the two-layered structure composed of the metal electrode and a portion of the contact electrode metal.

Subsequently, a silica passivation film of 300 nm was formed by printing and baking, using a sol-gel method, so as to cover the TFTs. Thereafter, using this silica passivation film pattern as a mask, portions of the i-type a-Si film and the SiN_x film on the gate electrode metal, which are to be connected to external driving circuitry, were etched away.

Finally, an Al–Zr alloy was once again vapor deposited on the entire surface to a film thickness of 150 nm, and using a photomask having a second comb-shaped electrode pattern, a second comb-shaped pixel metal electrode 282 was formed, thus producing a TFT array substrate 283 applicable to IPS mode transmissive liquid crystal display devices, with the use of three photomasks (Figs. 25(a) and 25(b)).

Consequently, because at least segments of each source segmented wiring line were connected together by the two-layered structure composed of the metal electrode and the contact electrode metal, it was possible to reduce the resistance of the source segmented wiring line, allowing fabrication of a TFT array substrate having excellent image display characteristics.

Example 2-12

The actual fabrication process of a liquid crystal display device using the TFT array substrate produced in the foregoing Example 2-11 is described.

First, there were provided a TFT array substrate, similar to that of Example 2-11, fabricated using two masks, more specifically, a first TFT array substrate including a first comb-shaped electrode group and a second comb-shaped electrode group arranged in a matrix and a transistor group that drives the first comb-shaped electrode group; and a second color filter substrate including a color filter group placed opposite to the first and second comb-shaped electrode groups. Over each of the substrates, by a conventional method, a polyimide resin was applied and cured, and the resulting films were subjected to rubbing, thus producing liquid crystal alignment films.

Next, the first and second substrates ~~and~~ were arranged such that their respective alignment films oppose one another, thus producing a cell having a gap of about 5 microns, which is created by spacers and adhesives. Thereafter, a TN liquid crystal was injected between the first and second substrates, and polarizers ~~and~~ were then arranged so as to have a crossed Nicols relation, thus completing a display device.

Such a device was capable of displaying images by driving each transistor using video signals while lighting, using the backlight from the backside. Here, the device achieved a wide viewing angle of 160° horizontally and vertically with a contrast of 10.

Here, after the step of fabricating the TFT array substrate prior to the formation of the alignment films, by carrying out the step of covering at least part of the TFT array substrate by a passivation film such as silica, it was possible to fabricate a liquid crystal display device with high reliability.